Specifications for the NI PXI/PCI-6552/6551

100/50 MHz Digital Waveform Generator/Analyzer

These specifications are valid for the operating temperature range, unless otherwise noted.

Channel Characteristics

Specification	Value	Comments
Number of data channels	20	—
Direction control of data channels	Per channel	—
Number of Programmable Function Interface (PFI) channels	4	Refer to the *Waveform Characteristics* section for more details.
Direction control of PFI channels	Per channel	—
Number of clock terminals	3 input 2 output	Refer to the *Timing Characteristics* section for more details.

NATIONAL INSTRUMENTS

Generation Signal Characteristics (Data, DDC CLK OUT, and PFI <0:3> Channels)

Specification	Value	Comments
Generation voltage range	–2.0 V to 5.5 V	Into 1 MΩ
Generation signal type	Single-ended	—
Number of programmable voltage levels	1 voltage low level 1 voltage high level **Note**: While you can only set one voltage low level and one voltage high level for all generation channels, you can set a different voltage low level and voltage high level for all acqusition channels.	For all data, CLK OUT (Sample clock only), and PFI channels
Generation voltage range restrictions	–0.5 V to 5.5 V (up to 50 MHz clock rate) –2.0 V to 3.7 V (up to 50 MHz clock rate) –0.5 V to 3.7 V (50 to 100 MHz clock rate; NI 6552 only)	Into 1 MΩ
Generation voltage swing	400 mV to 6 V (up to 50 MHz clock rate) 400 mV to 4.2 V (50 to 100 MHz clock rate; NI 6552 only)	Into 1 MΩ
Generation voltage level resolution	10 mV	Into 1 MΩ
DC generation voltage level accuracy	±20 mV	Into 1 MΩ; does not include system crosstalk
Output impedance	50 Ω nominal	At 25 °C
Output impedance temperature coefficient	0.2 Ω/°C	Typical
Maximum DC drive strength	±50 mA maximum per channel ±600 mA maximum for all data, clock, and PFI channels	—
Data channel driver enable/disable control	Per channel	Software-selectable

Specification	Value	Comments
Channel power-up state	Drivers disabled, 10 kΩ input impedance	—
Output protection	The device can indefinitely sustain a short to any voltage in the generation voltage range.	—

Acquisition Signal Characteristics (Data, STROBE, and PFI <0..3> Channels)

Specification	Value	Comments
Number of voltage comparators per channel	2	—
Acquisition voltage range	–2.0 V to 5.5 V	—
Number of programmable acquisition thresholds	1 voltage low threshold 1 voltage high threshold **Note**: While you can only set one voltage low level and one voltage high level for all acquisition channels, you can set a different voltage low level and voltage high level for all generation channels.	For all data, STROBE, and PFI channels
Minimum detectable voltage swing	50 mV	10 kΩ input impedance, measured with 50% duty cycle input signal
Acquisition voltage threshold resolution	10 mV	10 kΩ input impedance
DC acquisition voltage threshold accuracy	±30 mV	10 kΩ input impedance, does not include system crosstalk

Specification	Value	Comments
Input impedance	50 Ω nominal or 10 kΩ (default)	Software-selectable per channel, when powered on and within valid voltage range
Input protection	–2.3 V to 6.8 V	Diode clamps in the design may provide additional protection outside this range.

Timing Characteristics

Sample Clock

Specification	Value	Comments
Sample clock sources	1. On Board Clock (internal voltage-controlled crystal oscillator (VCXO) with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane—PXI only) 4. STROBE (DDC connector; acquisition only)	—
On Board Clock frequency range	**NI 6552**: 48 Hz to 100 MHz Configurable to 200 MHz/*N*, where $2 \le N \le 4{,}194{,}304$ **NI 6551**: 48 Hz to 50 MHz Configurable to 200 MHz/*N*, where $4 \le N \le 4{,}194{,}304$	—
CLK IN frequency range	**NI 6552**: 20 kHz to 100 MHz **NI 6551**: 20 kHz to 50 MHz	Refer to the *CLK IN (SMB Jack Connector)* section for restrictions based on waveform type.

Specification	Value		Comments
PXI_STAR frequency range (PXI only)	**NI 6552**: 48 Hz to 100 MHz **NI 6551**: 48 Hz to 50 MHz		Refer to the *PXI_STAR (PXI Backplane—PXI only)* section.
STROBE frequency range	**NI 6552**: 48 Hz to 100 MHz **NI 6551**: 48 Hz to 50 MHz		Refer to the *STROBE (Digital Data & Control (DDC) Connector)* section.
Sample clock relative delay adjustment	0 to 1 Sample clock period		You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	10 ps		
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)		Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range (δ_C)	0 to 1 Sample clock periods		For clock frequencies ≥25 MHz
Exported Sample clock delay resolution (δ_C)	1/256 of Sample clock period		For clock frequencies ≥25 MHz
Exported Sample clock jitter	Period Jitter	Cycle-to-Cycle Jitter	Typical; using On Board Clock
	20 ps_{rms}	35 ps_{rms}	

Generation Signal Characteristics (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value	Comments
Data channel-to-channel skew	±300 ps	Typical skew across all data channels
	±900 ps	Maximum skew across all data channels
Maximum data channel toggle rate	**NI 6552**: 50 MHz **NI 6551**: 25 MHz	—
Data formats	NRZ	—
Data position modes	Rising edge, Falling edge, or Delayed	Relative to Sample clock, per channel
Generation data delay range (δ_G)	0 to 1 Sample clock period	For clock frequencies ≥25 MHz
Generation data delay resolution (δ_G)	1/256 of Sample clock period	For clock frequencies ≥25 MHz

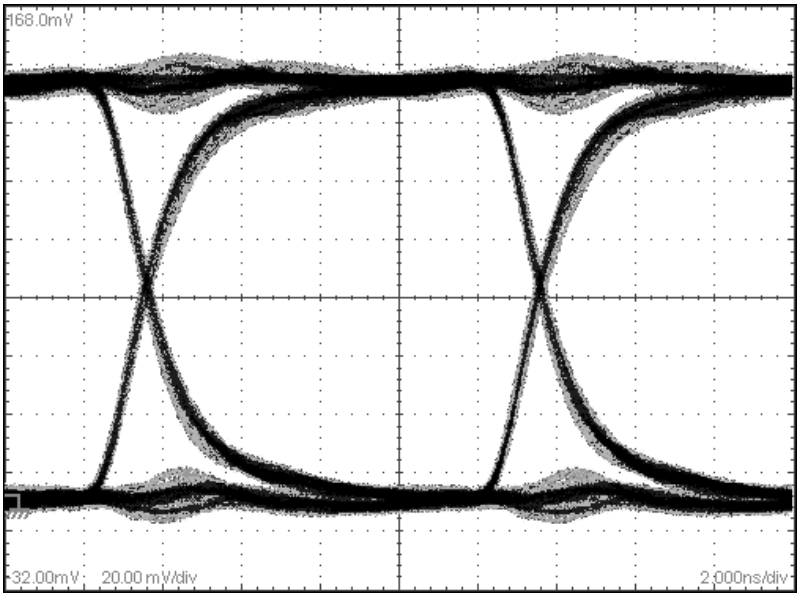
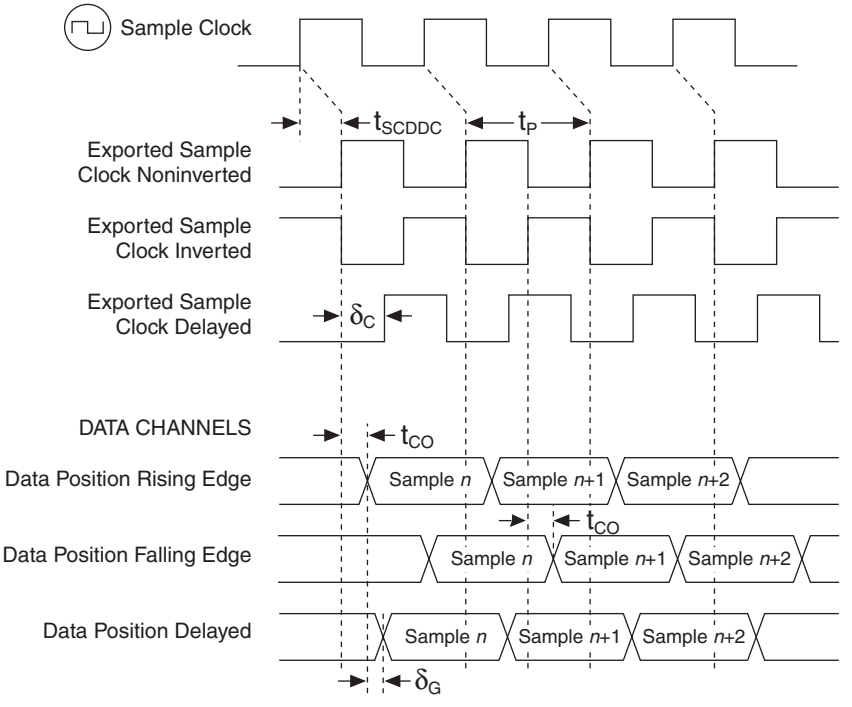


Figure 1. Eye Diagram[1]

Specification	Value		Comments
Rise time (0 V to 3.3 V swing)	Into 50 Ω	2.25 ns	20% to 80%, typical
	Into 1 MΩ	2.75 ns into 475 pF test system capacitance	
Fall time (0 V to 3.3 V swing)	Into 50 Ω	2.25 ns	20% to 80%, typical
	Into 1 MΩ	2.75 ns into 475 pF test system capacitance	
Exported Sample clock offset (t_{CO})	0 ns or 2.5 ns (default)		Software-selectable
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	32.5 ns		Typical

[1] This eye diagram was captured on DIO 0 (100 MHz clock rate) at 3.3 V at room temperature into 50 Ω termination.



t_{SCDDC} : Time delay from Sample Clock (internal) to DDC Connector

$0 \leq \delta_C \leq 1$: Exported Sample Clock Delay (fraction of t_P)

$0 \leq \delta_G \leq 1$: Pattern Generation Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

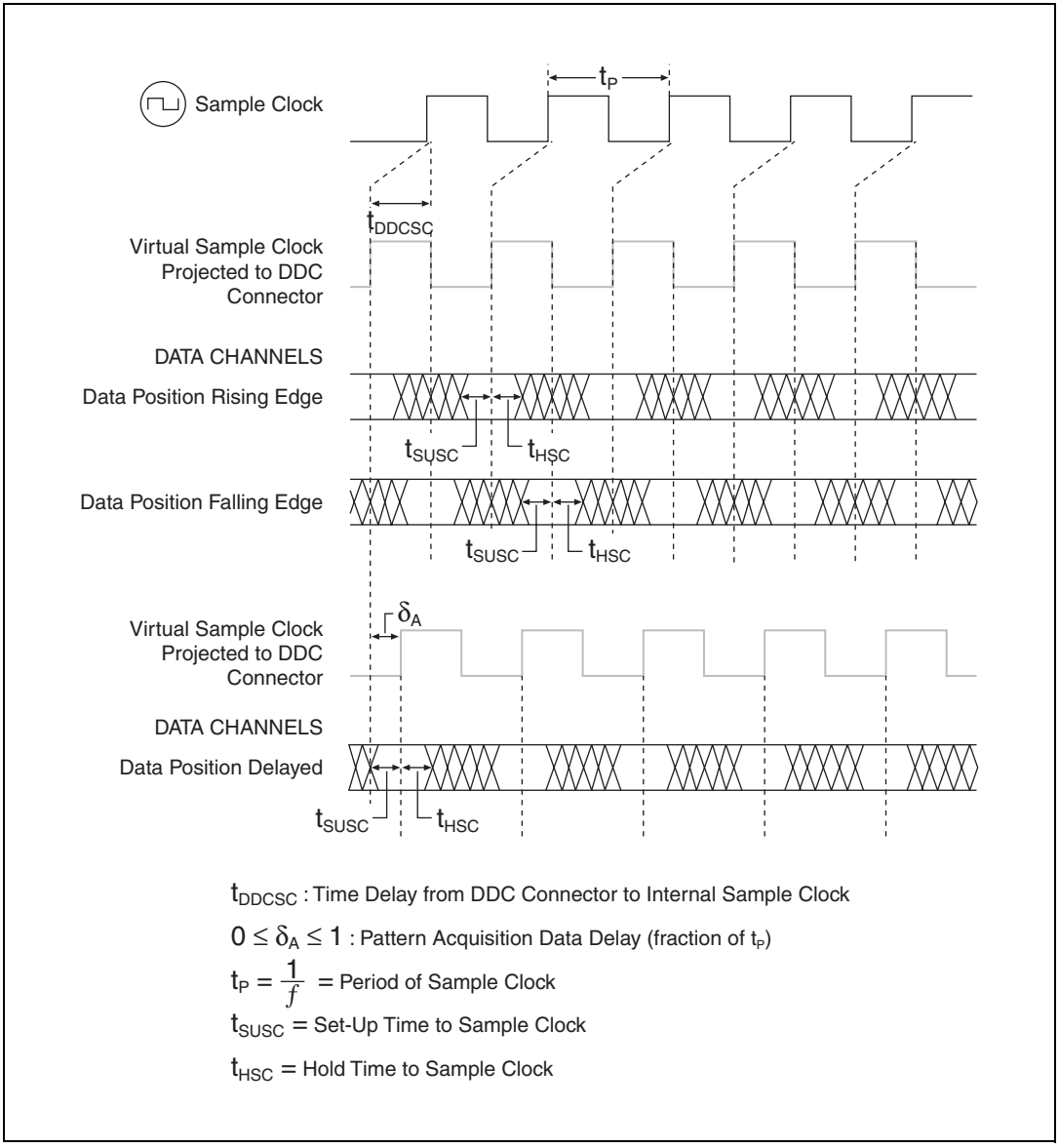
t_{CO} = Exported Sample Clock Offset; 0 or 2.5 ns, software-selectable

Figure 2. Generation Timing Diagram

Acquisition Signal Characteristics (Data, STROBE, and PFI <0..3> Channels)

Specification	Value	Comments
Channel-to-channel skew	±400 ps	Typical skew across all data channels
	±900 ps	Maximum skew across all data channels
Minimum detectable pulse width	4 ns	Required at both acquisition voltage thresholds
Set-up time to STROBE (t_{SUS})	2.3 ns	Maximum; includes maximum data channel-to-channel skew
Hold time to STROBE (t_{HS})	1.9 ns	Maximum; includes maximum data channel-to-channel skew
Time delay from DDC connector to internal Sample clock (t_{DDCSC})	27.5 ns	Typical
Set-up time to Sample clock (t_{SUSC})	0.4 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}

Specification	Value	Comments
Hold time to Sample clock (t_{HSC})	0 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Data position modes	Rising edge, Falling edge, or Delayed	Relative to Sample clock, per channel
Acquisition data delay range (δ_A)	0 to 1 Sample clock periods	For clock frequencies ≥25 MHz
Acquisition data delay resolution (δ_A)	1/256 of Sample clock period	For clock frequencies ≥25 MHz



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

Figure 3. Acquisition Timing Diagram

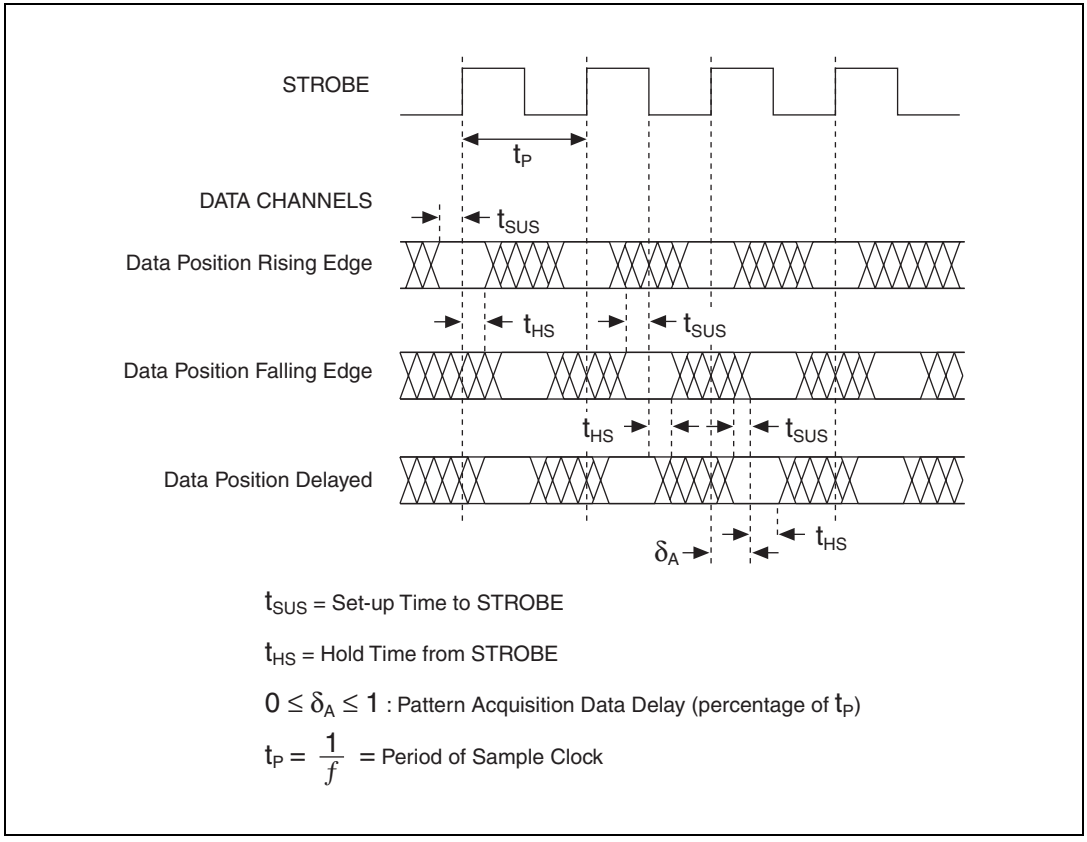


Figure 4. Acquisition Timing Diagram Using STROBE as the Sample Clock

CLK IN (SMB Jack Connector)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Reference clock (for the phase lock loop (PLL)) 2. Sample clock	—
Input coupling	AC	—
Input protection	±10 VDC	—
Input impedance	50 Ω (default) or 1 kΩ	Software-selectable

Specification	Value				Comments
Minimum detectable pulse width	4 ns				Required at V_{rms} mean
Clock requirements	Clock must be continuous and free-running				—
As Sample clock					
External Sample clock requirements	Square Waves				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}			—
	Frequency range	**NI 6552**: 20 kHz to 100 MHz			—
		NI 6551: 20 kHz to 50 MHz			—
	Duty cycle range	f < 50 MHz: 25% to 75% f ≥ 50 MHz: 40% to 60%			—
	Sine Waves				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	1.0 V_{pp} to 5.0 V_{pp}	2.0 V_{pp} to 5.0 V_{pp}	—
	Frequency range	**NI 6552**: 5.5 MHz to 100 MHz	**NI 6552**: 3.5 MHz to 100 MHz	**NI 6552**: 1.8 MHz to 100 MHz	—
		NI 6551: 5.5 MHz to 50 MHz	**NI 6551**: 3.5 MHz to 50 MHz	**NI 6551**: 1.8 MHz to 50 MHz	—
As Reference Clock					
Reference clock frequency range	10 MHz ±50 ppm				—
Reference clock voltage range	0.65 V_{pp} to 5.0 V_{pp}				—
Reference clock duty cycle	25% to 75%				—

STROBE (Digital Data & Control (DDC) Connector)

Specification	Value	Comments
Direction	Input into device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6552**: 48 Hz to 100 MHz **NI 6551**: 48 Hz to 50 MHz	—
STROBE duty cycle range	**NI 6552**: $f \leq 50$ MHz: 25% to 75% $f > 50$ MHz: 40% to 60% **NI 6551**: 40% to 60%	At the programmed thresholds
Minimum detectable pulse width	4 ns	Required at both acquisition voltage thresholds
Voltage thresholds	Refer to the *Acquisition Signal Characteristics (Data, STROBE, and PFI <0..3> Channels)* specifications in the *Channel Characteristics* section.	—
Clock requirements	Clock must be continuous and free-running	—
Input impedance	50 Ω or 10 kΩ (default)	Software-selectable

PXI_STAR (PXI Backplane—PXI only)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Sample clock 2. Start trigger 3. Pause trigger (generation sessions only) 4. Script trigger (generation sessions only) 5. Reference trigger (acquisition sessions only)	—

Specification	Value	Comments
PXI_STAR frequency range	**NI 6552**: 48 Hz to 100 MHz **NI 6551**: 48 Hz to 50 MHz	—
Clock requirements	Clock must be continuous and free-running	—

CLK OUT (SMB Jack Connector)

Specification	Value	Comments
Direction	Output	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω nominal	—
As Sample Clock		
Electrical characteristics	Refer to the *Generation Signal Characteristics (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Characteristics* section.	—
As Reference Clock		
Maximum drive current	24 mA	—
Logic type	3.3 V CMOS	—

DDC CLK OUT (Digital Data & Control (DDC) Connector)

Specification	Value	Comments
Direction	Output	—
Sources	Sample clock	STROBE cannot be routed to DDC CLK OUT
Electrical characteristics	Refer to the *Generation Signal Characteristics (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Characteristics* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK10 (PXI backplane—PXI only) 2. RTSI 7 (RTSI bus—PCI only) 3. CLK IN (SMB jack connector) 4. None (internal oscillator not locked to a reference)	Provides the reference frequency for the phase lock loop
Lock time	400 ms	Typical
Reference clock frequencies	10 MHz ±50 ppm	—
Reference clock duty cycle	25% to 75%	—
Reference clock destinations	CLK OUT (SMB jack connector)	—

Waveform Characteristics

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 655*X* uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size	1 Mbit/channel (for generation sessions) 1 Mbit/channel (for acquisition sessions)	8 Mbit/channel (for generation sessions) 8 Mbit/channel (for acquisition sessions)	64 Mbit/channel (for generation sessions) 64 Mbit/channel (for acquisition sessions)	Maximum limit for generation sessions assumes no scripting instructions.

<table>
<tr><th>Specification</th><th>Value</th><th>Comments</th></tr>
<tr><td>Generation modes</td><td>Single-waveform mode:
Generate a single waveform once, N times, or continuously.

Scripted mode:
Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.</td><td>—</td></tr>
<tr><td>Generation minimum waveform size</td><td><table><tr><th rowspan="2">Configuration</th><th colspan="2">Sample Rate</th></tr><tr><th>100 MHz
(NI 6552 only)</th><th>50 MHz</th></tr><tr><td>Finite waveform</td><td>2</td><td>2</td></tr><tr><td>Continuous waveform</td><td>32</td><td>16</td></tr><tr><td>Stepped triggered script</td><td>128</td><td>64</td></tr><tr><td>Burst triggered script</td><td>512</td><td>256</td></tr></table></td><td>Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.

For information on these configurations, refer to the Common Scripting Use Cases topic in the NI Digital Waveform Generator/ Analyzer Help.</td></tr>
<tr><td>Generation finite repeat count</td><td>1 to 16,777,216</td><td>—</td></tr>
<tr><td>Generation waveform quantum</td><td>Waveform size must be an integer multiple of two samples.</td><td>Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.</td></tr>
</table>

Specification	Value	Comments
Acquisition minimum record size	1 sample	—
Acquisition record quantum	1 record	—
Acquisition number of pre-Reference trigger samples	0 up to full record	—
Acquisition number of post-Reference trigger samples	0 up to full record	—

Triggers (Inputs to the NI 655*X*)

Specification	Values	Comments
Trigger types	1. Start trigger 2. Pause trigger 3. Script trigger (generation sessions only) 4. Reference trigger (acquisition sessions only)	—
Sources	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only) 4. PXI_STAR (PXI backplane—PXI only) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)	—

<table>
<tr><th>Specification</th><th colspan="2">Values</th><th>Comments</th></tr>
<tr><td>Trigger detection</td><td colspan="2">1. Start trigger (edge detection: rising or falling)
2. Pause trigger (level detection: high or low)
3. Script trigger (edge detection: rising or falling; level detection: high or low)
4. Reference trigger (edge detection: rising or falling)</td><td>—</td></tr>
<tr><td>Minimum required trigger pulse width</td><td colspan="2">30 ns</td><td>Acquisition triggers must meet set-up and hold time requirements.</td></tr>
<tr><td>Destinations</td><td colspan="2">1. PFI 0 (SMB jack connectors)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)</td><td>Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.</td></tr>
<tr><td rowspan="2">Delay from Pause trigger to Paused state</td><td>Generation Sessions</td><td>Acquisition Sessions</td><td>—</td></tr>
<tr><td>32 Sample clock periods + 150 ns</td><td>Synchronous to the data</td><td>Use the Data Active event during generation to determine when the NI 655X enters the Paused state.</td></tr>
<tr><td>Delay from trigger to digital data output</td><td colspan="2">32 Sample clock periods + 160 ns</td><td>—</td></tr>
</table>

Events (Output from the NI 655*X*)

Specification	Value	Comments
Event type	1. Marker (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event	—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)	Each event, except the Data Active event, can be routed to any destination. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers must be placed at an integer multiple of two samples.	—

Calibration

Specification	Value	Comments
Interval for external calibration	2 years	—
Warm-up time	15 minutes	—
Onboard calibration voltage reference		
Temperature coefficient	±5 ppm/°C	—
Long-term stability	90 ppm/$\sqrt{\text{kHr}}$	Typical
On Board Clock characteristics (only valid when PLL reference source is set to None)		
Frequency accuracy	±100 ppm	Typical

Specification	Value	Comments
Temperature stability	±30 ppm	Typical
Aging	±5 ppm first year	Typical

Power

Specification	Value			Comments
	Typical	Maximum		
+3.3 VDC	2.0 A	2.0 A		—
+5 VDC	1.8 A	PXI	PCI	—
		2.3 A	2.4 A	—
+12 VDC	0.3 A	0.5 A		—
–12 VDC	0.2 A	0.2 A		—
Total power	21.6 W	PXI	PCI	—
		26.5 W	27 W	—

Software Specifications

Specification	Value	Comments
Driver software	NI-HSDIO driver software. NI-HSDIO allows you to configure, control, and calibrate the NI 655*X*. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI API guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments: • National Instruments LabVIEW 7.0 or later • National Instruments LabWindows™/CVI™ 6.0 or later • Microsoft Visual C/C++ 6.0 or later	—
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 655*X*. MAX is included on the NI-HSDIO driver CD.	—

Physical Specifications

Specification	Value		Comments
Dimensions	**PXI**: 18.6 cm × 13.1 cm (7.32 in. × 5.16 in.) Single 3U CompactPCI slot; PXI compatible **PCI**: 12.6 cm × 35.5 cm (4.95 in. × 13.9 in.)		—
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CLK IN	External Sample clock, external PLL reference input	SMB jack connector	—
PFI 0	Events, triggers	SMB jack connector	—
CLK OUT	Exported Sample clock, exported Reference clock	SMB jack connector	—
DIGITAL DATA & CONTROL	Digital data channels, exported Sample clock, STROBE, events, triggers	68-pin VHDCI connector	—

Environment and Compliance

Specification	Value	Comments
Operating/ storage environment	Indoor use only	—
Operating temperature	**PXI**: 0 ºC to +55 ºC in all NI PXI chassis except the following: 0 ºC to +45 ºC when installed in an NI PXI-1000/B and NI PXI-101*X* chassis (Meets IEC-60068-2-1 and IEC-60068-2-2) **PCI**: 0 ºC to +45 ºC	—
Storage temperature	–20 °C to 70 °C	—
Operating relative humidity	10% to 90% relative humidly, noncondensing (Meets IEC-60068-2-56)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC-60068-2-56)	—

Specification	Value	Comments
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	NI PXI-655*X* only
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	NI PXI-655*X* only
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC-60068-2-64)	NI PXI-655*X* only
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B)	NI PXI-655*X* only
Altitude	0 m to 2000 m above sea level (at 25 ºC ambient temperature)	—
Pollution Degree	2	—
Safety	The NI 655*X* meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 3111-1, UL 61010B-1 • CAN/CSA C22.2 No. 1010.1	For UL and other safety certifications, refer to the product label or to `ni.com`.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant **Note**: For EMC compliance, you *must* operate this device with shielded cabling.	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—

Specification	Value	Comments
Electro-magnetic Compatibility Directive (EMC)	89/336/EEC	—
For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/hardref.nsf`, and search by model number or product line, and click the appropriate link in the Certification column.		

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